

DATA COLLECTION OPERATIONAL SUPPORT SYSTEM
PART I

William R. Woughter, Jr.

Federation of Rocky Mountain States, Inc.
2480 W. 26 Ave. Suite 300B
Denver, Colorado 80211

November, 1975

Final Report

Prepared for:

Goddard Space Flight Center
Greenbelt, Maryland 20771

TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No. NAS5-20533	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle DATA COLLECTION OPERATIONAL SUPPORT SYSTEM - FINAL REPORT, PART I		5. Report Date NOVEMBER, 1975	6. Performing Organization Code
7. Author(s) William R. Woughter, Jr.	8. Performing Organization Report No.		10. Work Unit No.
9. Performing Organization Name and Address Federation of Rocky Mountain States 2480 W. 26 Ave. Suite 300B Denver, Colo. 80211		11. Contract or Grant No. NAS5-20533	13. Type of Report and Period Covered Final Report
12. Sponsoring Agency Name and Address Mr. E. L. Harper Code 951 GSFC Greenbelt, Md. 20771		14. Sponsoring Agency Code	
15. Supplementary Notes Appendix A written by Harold F. Huntsman			
16. Abstract The Data Collection Operational Support system has been shown to be a useable means of transmitting numerical data over a 2-way VHF satellite link. It is also capable of supporting educational applications. This report details the design, operation, use, results, and recommendations of the system.			
17. Key Words (Selected by Author(s)) Data collection & transmission, Digital design, VHF communication, Computer programming, Interactive learning		18. Distribution Statement	
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 33	22. Price*

*For sale by the Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151.

PREFACE

The objective of this contract was to design, implement, and operate a data collection system for the real-time collection of signal strength readings and climatic conditions. This data was to be collected from two-way audio satellite terminals operating in the Rocky Mountain region as part of the ATS-6 Health-Education-Telecommunications (HET) project.

The design proceeded from a prototype of one poller and twelve keypads to a final version. The poller was designed for inclusion in the existing digital circuitry of the remote VHF sites. Paramount to the proper operation of the system was the preparation of a computer program for the on-line minicomputer at the network center.

This report details the design, operation, use, and results of the Data Collection Operational Support (DCOS) system.

The DCOS system has been shown to be a useful means of transmitting numerical data over a 2-way VHF satellite link. It is also capable of supporting educational applications. Testing, although not as extensive as planned, did show the system to be both workable and an enhancement for the learning process when used with educational programming.

It is recommended that extended and related applications for this system be explored. Further technical improvements, redesigns, and added features are also recommended.

The author wishes to gratefully acknowledge the encouragement and direction given by Dail Ogden, a pioneer in the field of educational keypads. Particular appreciation is extended to Dennis Laurence and Dr. James Janky for their valuable contributions to this effort.

TABLE OF CONTENTS

1.0	INTRODUCTION	p. 1
1.1	THE STD NETWORK	p. 1
1.2	THE DCOS SYSTEM	p. 1
2.0	PROTOTYPE SYSTEM	p. 3
3.0	FINAL DCOS SYSTEM	p. 5
3.1	KEYPAD DESIGN	p. 5
3.2	POLLER DESIGN	p. 12
4.0	DCOS OPERATION	p. 30
4.1	NETWORK CENTER FUNCTION	p. 30
4.2	SITE FUNCTION	p. 31
5.0	DCOS FIELD TESTING & USE	p. 31
6.0	RESULTS, CONCLUSIONS, & RECOMMENDATIONS	p. 32

LIST OF ILLUSTRATIONS

Figure 1	KEYPAD (picture)	p. 6
Figure 2	KEYPAD CIRCUIT BOARD (picture)	p. 7
Figure 3	KEYPAD SCHEMATIC	pp. 8, 9
Figure 4	KEYPAD SCHEMATIC	p. 10
Figure 5	SYSTEM BLOCK DIAGRAM	p. 13
Figure 6	POLLER CIRCUIT BOARD (picture)	p. 14
Figure 7	POLLER BOARD LAYOUT	p. 15
Figure 8	DIGITAL COORDINATOR (picture)	p. 16
Figure 9	COMMAND DECODING & LATCHES	p. 18
Figure 10	KEYPAD INTERFACE - B	p. 19
Figure 11	PROGRAM & ADDRESS GENERATOR	pp. 20, 21
Figure 12	KEYPAD INTERFACE - A	p. 22
Figure 13	MEMORY	p. 23
Figure 14	TIMING & CONTROL	p. 24

1.0 INTRODUCTION

1.1 THE STD NETWORK

The Broadcast and Engineering component of the Satellite Technology Demonstration (STD), a part of the ATS-6 Health/Education Telecommunications (HET) experiment, was responsible for designing, implementing, and maintaining a complex network of satellite telecommunications ground terminals. Consisting of a mixture of S-band and VHF equipment, the system included 45 S-band receive-only terminals plus 24 intensive terminals equipped with both S-band receivers and VHF transceivers. Since 2-way S-band transmission was not possible due to regulatory difficulties, the VHF facilities were added to give the intensive sites a 2-way capability.

Although the VHF equipment at each intensive site was used predominantly in a 2-way audio mode, the VHF terminal was controlled by a device called the digital coordinator. This unit performed the actual transmitter keying, receiver muting, channel selection, voice/data mode selection, and other tasks. The coordinator transmitted and received binary ASCII encoded information at 1200 baud over the VHF channel. Each transmission from a remote site, whether audio or data, was preceded by a five byte preamble containing site identification and mode of operation information. Reception of digital information at a site evoked a response from the coordinator only if the transmission was addressed to that site. An on-line minicomputer was provided at the Network Coordination Center (NCC) to maintain efficient VHF network discipline in both audio and data modes. The computer's role was to process information and requests for service from the remote sites, and in turn to transmit appropriate commands to individual sites.

1.2 THE DCOS SYSTEM

Shortly before the STD network went into the operational stage, NASA awarded a contract to the Federation of Rocky Mountain States, parent organization of the STD, for development of a Data Collection Operational Support (DCOS) system. This system was planned to facilitate collection of signal strength, weather, site status, and other related data in real time. Such data was considered useful both to STD staff and to NASA for ATS-6 link evaluation and satellite pointing operations. The flexible design of the digital coordinator permitted expansion of its capabilities to encompass the DCOS system. The following paragraphs outline the concept, objectives, and ancillary considerations of the system.

The digital coordinator can accept external data and transmit it in a bit-serial stream. Consequently one or more limited data entry terminals, called keypads, may be interfaced to the coordinator for data transmission. In this context "limited" denotes the ability of the keypads to enter only numeric rather than alphanumeric data. (A full alphanumeric version

could have been made had the added expense been considered worthwhile.)

The keypads are provided with a single-digit display for verification of the keypad operator's entry. In addition, three indicators present "ready," "right," and "wrong" feedback to the operator.

Each keypad is assigned a number and will only transfer data when it is electronically addressed by its number. Use of this characteristic permits polling a number of keypads; that is, collecting data sequentially from each keypad. This also allows connection of the keypads to the coordinator via a common bus rather than using individual cables. Identification of the response from any one keypad may be made at the network center by noting the position of the response in the data sequence.

In addition to making the described system operational, one goal is to make operation as simple as possible. Since all functions are under control of the network center computer, operation appears virtually automatic to the user. His only requirement is to enter data at the appropriate times.

The choice of a digital mode as opposed to the existing audio mode appears preferable for the DCOS function for several reasons:

- 1) It presents numeric data, suitable for processing by a computer, rather than subjective comments.
- 2) Collection of data by digital techniques can be accomplished in much less time than by oral polling.
- 3) Operation of the system is silent, allowing it to be used during video programming without disturbing the audience.
- 4) The likelihood of errors or lost data is reduced.
- 5) All large numbers of users can enter data into the system simultaneously, and at their convenience, rather than one at a time as polled over the audio system.
- 6) The audio system can be used as a backup for data transfer in the event the digital system were to be inoperative.
- 7) The heart of a digital data link, the digital coordinator, is already available in the system.

In the case of data collection, as envisioned in the original scope of this work, a benefit arises from the close association with a computer at the network center. In this case computations may be performed using the collected data to obtain direct information such as satellite pointing errors, effects of various weather conditions, statistical measures and correlations of various kinds, as well as other

items of interest. These computations take on greater impact as they are generated in approximately real time--that is, within as little as a few seconds after the readings are taken.

While the original scope of this work was limited to one form of data collection, the basic concept is of a broader nature. A system of multiple, polled keypads, remotely controlled, can provide a versatile basis for human interface to a host of technology-based services. In addition to data collection, such a system's 2-way nature permits measurement of individual responses including opinions, acceptance of programming, and retention of material presented. It may also be the key to providing remote site personnel access to various computer-based services. Imagine, for example, a teacher sending the "key" to an exam to the computer center via one of the keypads. During class time the exam could be given, this time using the keypads to record the students' responses. The computer would grade the individual's results, compute a median grade and standard deviation, and transmit the results back to the teacher. In other cases a doctor might request a computer readout of a patient's medical history, a professor would be able to record and read back students' grades, and a local law enforcement officer could request important data from a statewide data bank.

In consideration of the classroom environment of the VHF STD sites, the system has been designed to also accommodate educational applications. This report details the development, final design, and operation of the DCOS system along with pertinent conclusions and recommendations.

2.0 PROTOTYPE SYSTEM

Initially two consultants were retained to develop the keypad and polling circuitry. Twelve keypads and one poller were to be fabricated for testing as a prototype system. Based on findings from this testing, design changes were made as necessary and the final system fabricated.

The keypads incorporated twelve switch capsules for pushbuttons, three status lights, and a numeric display on a printed circuit board mounted in a clear plastic case. The outside dimensions were 15.3 cm (6 in) length and width by 2 cm (0.8 in) thick, with a weight of 0.28 kg (10 oz). The buttons were numbered 0 - 9 with two additional symbols - and · (displayed as A and F, respectively, due to the nature of the seven segment display.)

The keypad circuit board had two 24-contact edge connectors, one of which fed signals to and from the keypad, while the other fed the same signals to and from succeeding pads. Thus all keypads in any single installation were connected in series, with the option of connecting additional pads or disconnecting existing ones at any time. The order of connecting the pads with respect to their numeric information addresses could be completely random. A 5-wire bus fed address information to all the keypads, a 4-wire bus collected data from the

keypads, and three other wires transmitted timing and status information. The address of a specific keypad could be modified by replacing a plug-in address card.

Original logic on the keypad circuit board forced either the "right" or "wrong" indicator to be on whenever power was applied. In addition the "ready" light, which indicated when data entry was appropriate, remained on during the polling sequence. To correct this, the engineering staff modified the design and retrofitted the circuit boards prior to system testing to allow either light to be on only at the appropriate time and to prohibit more than one of the three ("ready," "right," and "wrong") indicators to be on at any one time. Also the capability of locking the current response into the keypad was added, preventing any change being made from the keyboard.

The polling circuitry provided by one of the consultants served as a basis for further work. However, to accommodate changes in the desired data format and to interface with the coordinator the poller was redesigned by a member of the engineering staff.

The poller was able to receive several commands from the network's center. One of these would turn on the "ready" indicators. Another set of commands started the polling sequence. Encoded in each of these commands was the correct answer to which the answer from each keypad was compared. The resulting "right" or "wrong" indication was displayed for approximately 15 seconds while the keypad was locked to further entries. This function was determined by a timer in the poller. Another command encoded information to inhibit this timer and to disable the "right"/"wrong" feedback.

The polling sequence consisted of addressing each of the 28 possible keypad locations in reverse order (beginning with #28 and ending with #1) in two consecutive passes to provide for error checking. The data from the keypads were collected and transmitted as each one was addressed.

Assuming that a site had only one keypad, (as would have been the case at most sites) only one digit at a time could be sent using the prototype system without the network center initiating a new polling sequence. This would have resulted in a cumbersome procedure for sending a series of digits as would have been required in overall site status reporting. Therefore, a modified design for the polling unit was undertaken to permit storage of a series of digits from one keypad for transmission as a block of data.

The prototype system was operated successfully with the radio link being simulated. Later a teletype was interfaced to the system. A staff member of the STD research component took the latter combination to two schools for field testing of the educational capabilities of the system.

3.0 FINAL DCOS SYSTEM

3.1 KEYPAD DESIGN

The production model keypad shown in figures 1 & 2 has dimensions of 20.2 cm (8 in) x 12.4 cm (4.9 in) x 6.0 cm (2.4 in) with a weight of 0.33 kg (11.5 oz) exclusive of cabling. It is housed in a molded plastic case and contains the display and keyboard features of the prototype model. One exception is the lettering of the two non-numeric keys as * and # (still displayed as A and F, respectively, due to the nature of the seven segment display.)

The button switches used as keys in the prototype model gave trouble with erroneous data entry due to contact bounce complicated by factors in the initial circuit design. Hence a sealed conductive elastomer keyboard is used in the production model. However, this unit has a higher "on" resistance and a variable turn-on rise time, necessitating use of Schmitt trigger inverters IC-4 and 16 (ref. Keypad Schematics, figures 3 and 4) to buffer and debounce the keyboard switch closures. The Schmitt trigger outputs are encoded to give a 4-wire binary equivalent of the entry digit. The encoder is made up of four groups of NOR gates and inverters from IC-2, 5, 6, and 17. The NOR gate outputs in each group are connected in a wired-AND configuration, followed by an inverter. The composite gate thus formed is equivalent to a large OR gate. The outputs of the composite gates appear at IC-2 pins 4, 6, 12, and 10 with binary weights of 1, 2, 4, and 8, respectively.

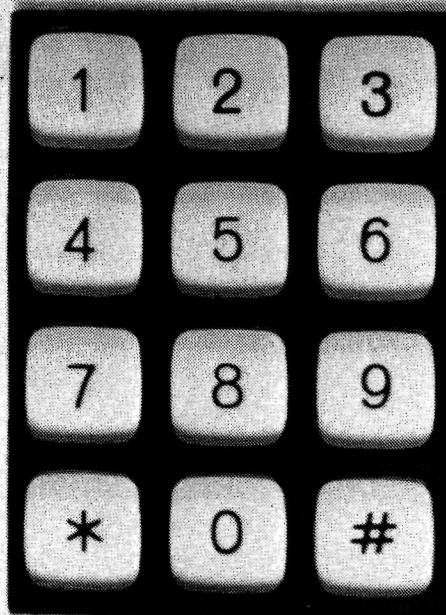
Each OR gate's output plus the 0 key Schmitt trigger signal is OR'd in a similar composite OR gate structure whose output appears at IC-2 pin 8. This output goes to a high level whenever any key is depressed. An edge detecting pulse generator gives a negative pulse out at the leading edge of this key-depressed signal. The edge detecting pulse generator is formed by an inverter from IC-2, a NAND gate from IC-1, and capacitor C3. This pulse is inverted at pin 6 of IC-14 to form the positive pulse which causes the four lines of binary data to be entered into the register IC-8. The latched outputs of IC-8 drive the display decoder IC-12 which drives the display IC-10.

IC-8's outputs also feed the four three-state drivers in IC-9. These drivers only pass the data to the data bus when the keypad is being addressed and consequently a low signal is present at IC-9 pins 1, 4, 10, and 13. Current limiting resistors R1, R2, R6, and R10 form protection for the drivers should more than one keypad accidentally enable their drivers at the same time.

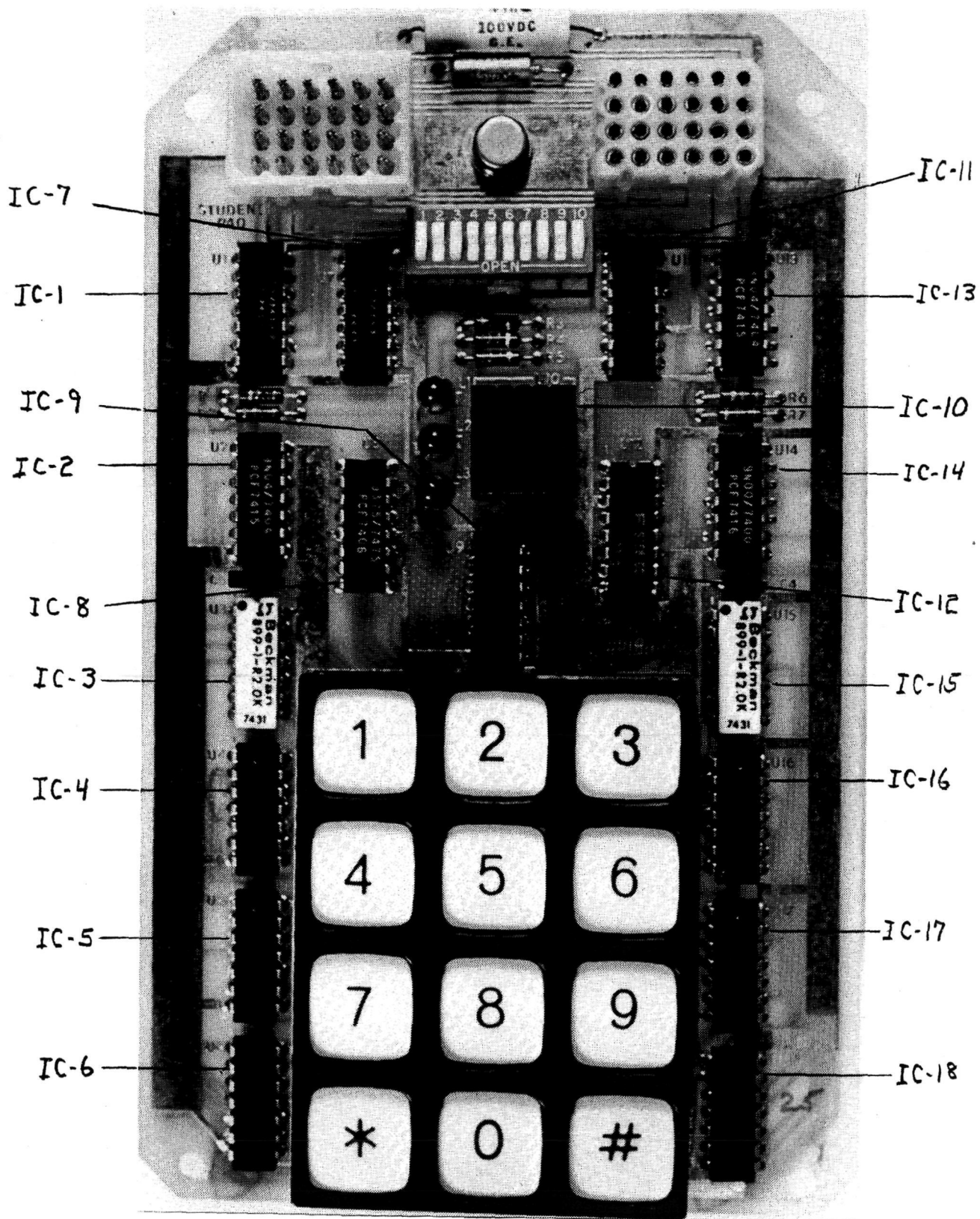
The negative "key depressed" pulse at IC-1 pin 6 is further gated through two stages of IC-18 by the low level "address recognized" signal at IC-18 pin 3. This pulse becomes the "multi-digit entry clock" signal which is returned to the poller.

FEDERATION OF
ROCKY MOUNTAIN STATES

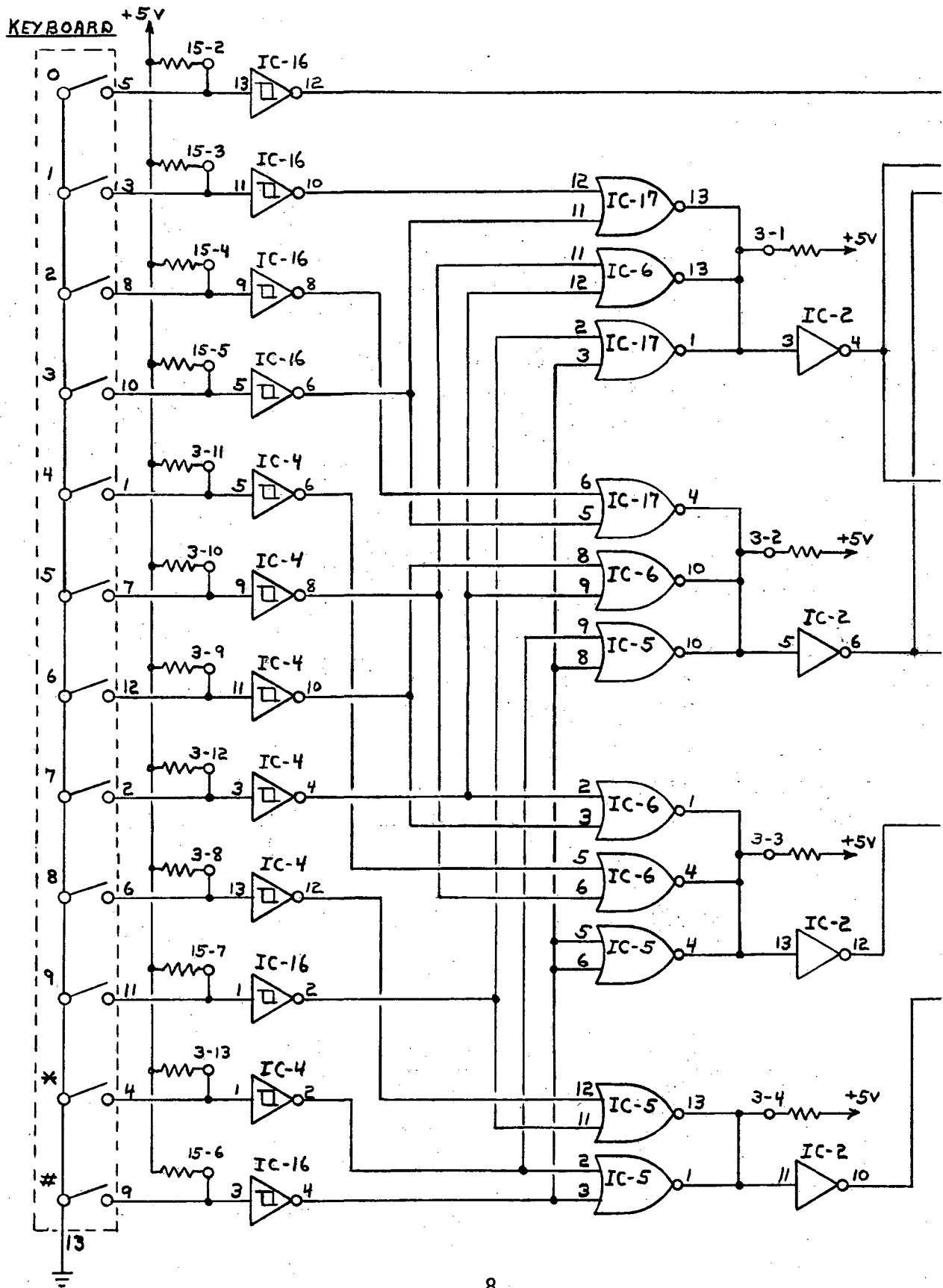
WRONG
READY
RIGHT

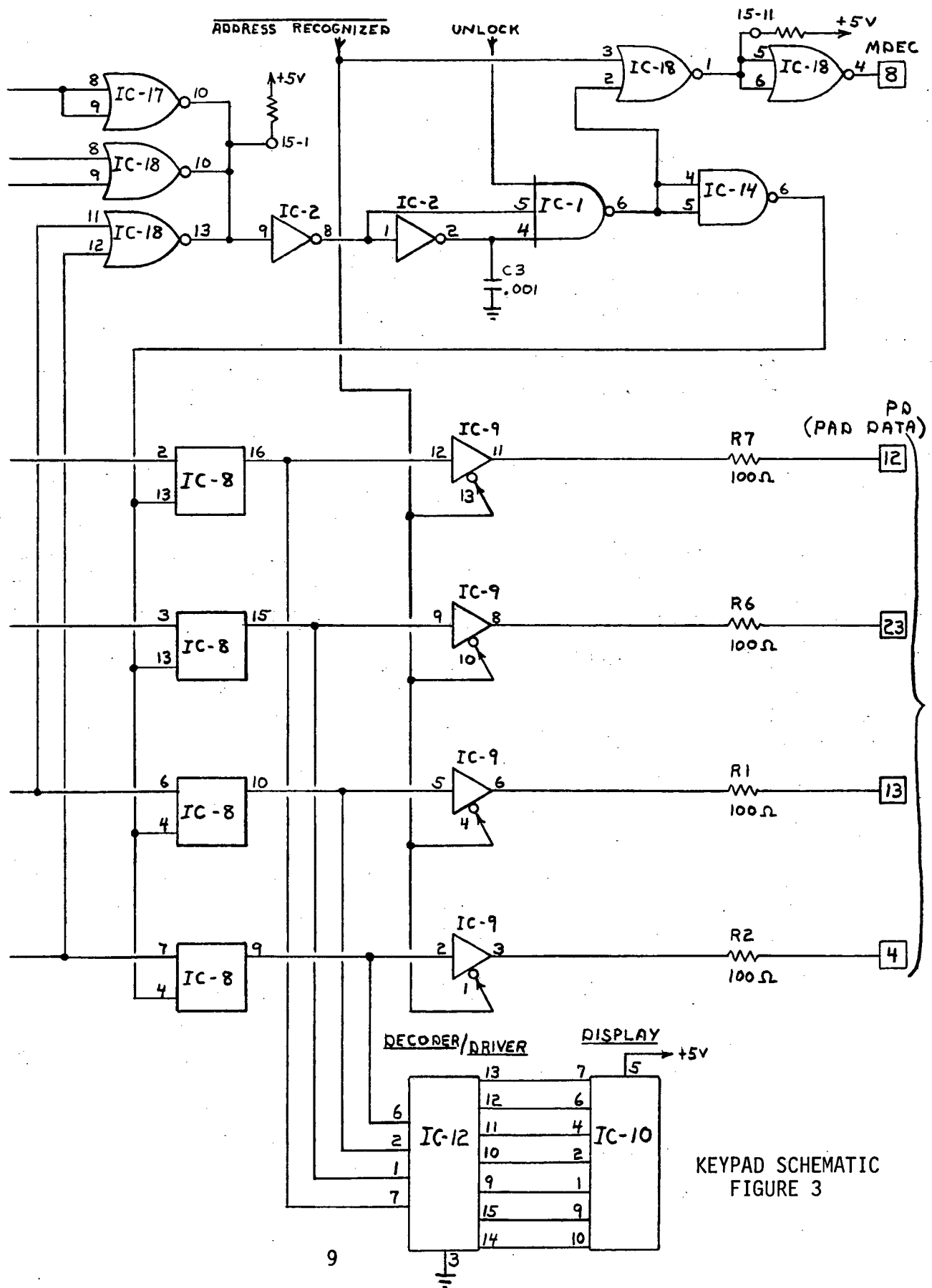


PRODUCTION KEYPAD, FIGURE 1



KEYPAD CIRCUIT BOARD, FIGURE 2





The address selection and recognition function of the keypad is performed by inverters IC-13, NAND gate IC-7, and the ten dual-inline packaged switches. The five lines of the address bus and the inverse signals of those lines are connected to one pole of each of the ten switches. The other poles of the switches are wired in groups of two switches. One and only one switch in any group of two is to be closed at a given time. The instructions for setting the switches for a desired address are given in appendix A. When the signals on the address bus are such that NAND gate IC-7 sees high levels on all its inputs, its output on pin 8 goes low, indicating recognition of the pad's address. This signal enables the data drivers to send the current entry back to the poller, and allows the "multi-digit entry clock" pulse to be returned to the poller, in the event the multi-digit mode is in use.

The low level "address recognized" signal is also inverted at pin 3 of IC-14 to provide a high level "address recognized" enable to pin 10 of IC-14. Through this NAND gate the feedback clock pulse from the poller is enabled to clock the two flip-flops in IC-11. Depending on the level from the poller at the D inputs of the flip-flops, the "right" or "wrong" light turns on at the time of the clock pulse.

The ability to lock the keypad display begins with the detection of an "unlock" condition at NAND gate pin 8 of IC-1. "Unlock" arises from a special address signal outside the allowable range of keypad addresses, such that all lines of the address bus are high. This corresponds to the address 32. (Note: The binary value is actually represented by the number 31. This is due to the fact that the pads are numbered 1 to 28 while the poller actually addresses binary equivalents of 0 to 27. Pad #1 is binary 0, pad #2 is binary 1, etc. This was done to avoid having a pad numbered "0".) The "unlock" signal is always present except during the time-out of the feedback timer in the poller or during the actual polling interval, with the further exception that it is present during the multi-digit polling (transmission from memory).

The "unlock" signal is applied to the set and reset pins 4 and 13 of IC-11 to hold the "right" and "wrong" indicators off when the pad is unlocked. Capacitor C5 prevents fast transitions on the address bus from accidentally turning off the indicators during the remainder of polling.

The inverted "unlock" signal at pin 6 of IC-13 is used at pin 13 of IC-14 to turn off the ready indicator during polling and the feedback locked period. It also provides the enable at IC-1 pin 13 for the data entry pulse during the unlocked period.

Power to the unit can be unregulated +8 to +12 VDC since a +5 V regulator, Q1, is incorporated in the keypad. Power and signal connections are made through a 24 conductor cable. The keypad has two 24 pin Molex connectors, one male and one female. Should one keypad fail, it

could be disconnected from the system and the male and female connectors on its cables could be connected to continue the series.

The mechanical design of the keypad is such that by adding a simple gasket around the keyboard (possibly a bead of silicone rubber) the unit could be made virtually immune to damage from spilled liquids, broken pencil leads, etc.

3.3.2 POLLER DESIGN

The poller circuitry is completely contained on one printed circuit card 20.2 cm (8 in) x 14 cm (5.5 in) shown in figures 6 & 7. The card contains 39 dual-inline circuit packages plus 35 discrete components. It plugs into the seventh card slot in the digital coordinator and requires two additional ribbon cables having 16 pin dip plugs to complete the connections to the coordinator (see fig. 8). A 24 pin Molex connector is mounted at the top of the card for connections to the keypads. Two machine screw/nut assemblies are mounted next to the Molex connector, and accept two wires with spade lug terminations as leads for the unregulated power supply to the keypads.

A block diagram of the poller connected in the system is shown in figure 5. Operations begin at the "Received Byte 3" port of the coordinator. Commands from this port are decoded and stored in the "Command Decoding & Latches" section, which in turn instructs the other sections as to procedures. This section also presents information via the "Correct Answer Bus" to the "Interface B" section where it is used for right/wrong comparison with individual keypad responses.

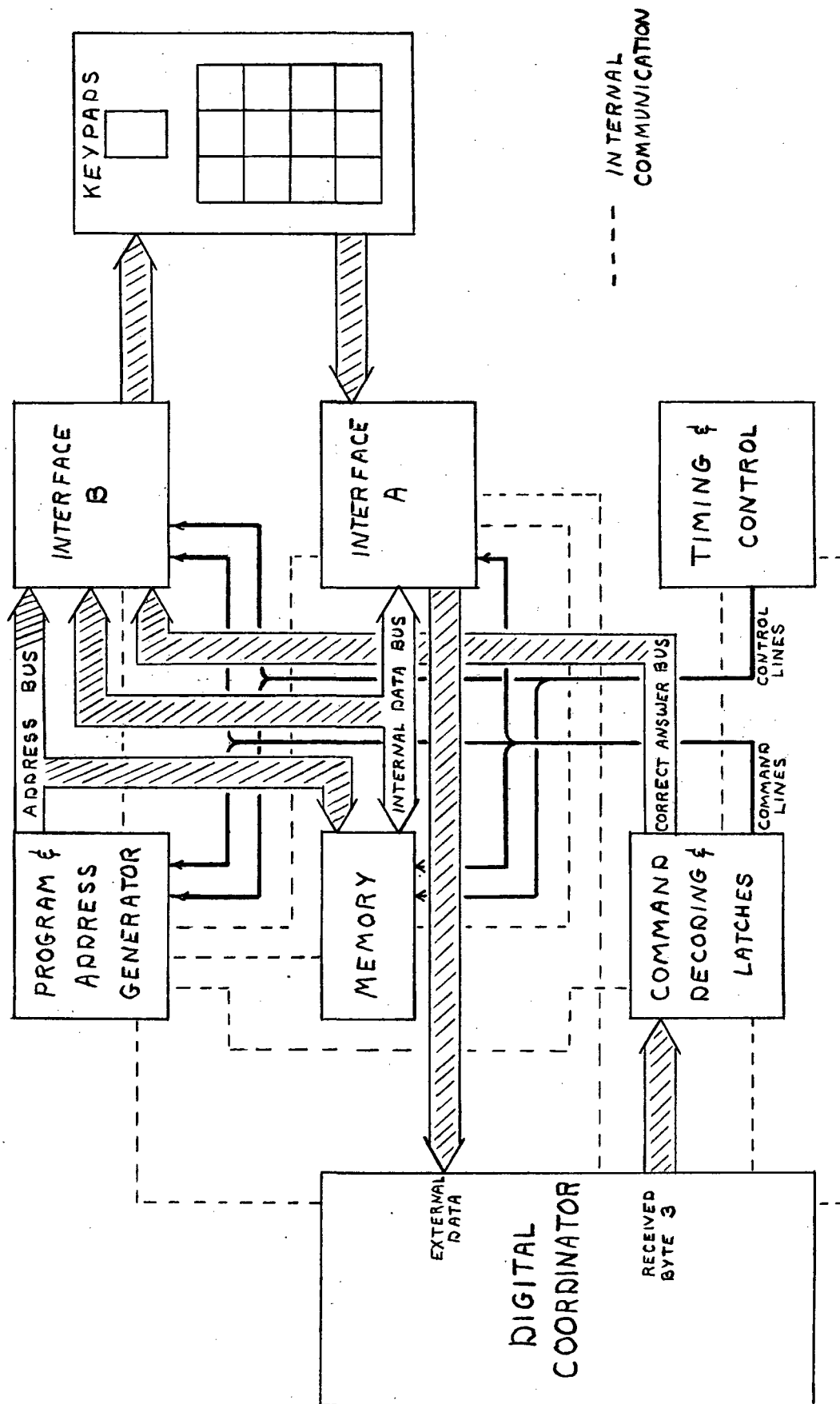
The "Timing & Control" section causes the instructions to be executed in the proper time relationship. It interfaces also with the coordinator in relation to when the coordinator can accept more data, and when it is available from the poller.

"Interface A" is the section which handles all information returning from the keypads. It in turn presents data to the coordinator at the "External Data" port for transmission. It also communicates with the ANSWER COMPARATOR in "Interface B" via the 2-way "Internal Data Bus."

The "Memory" section also communicates over the "Internal Data Bus" both to receive data from the master keypad and to transmit it to the coordinator.

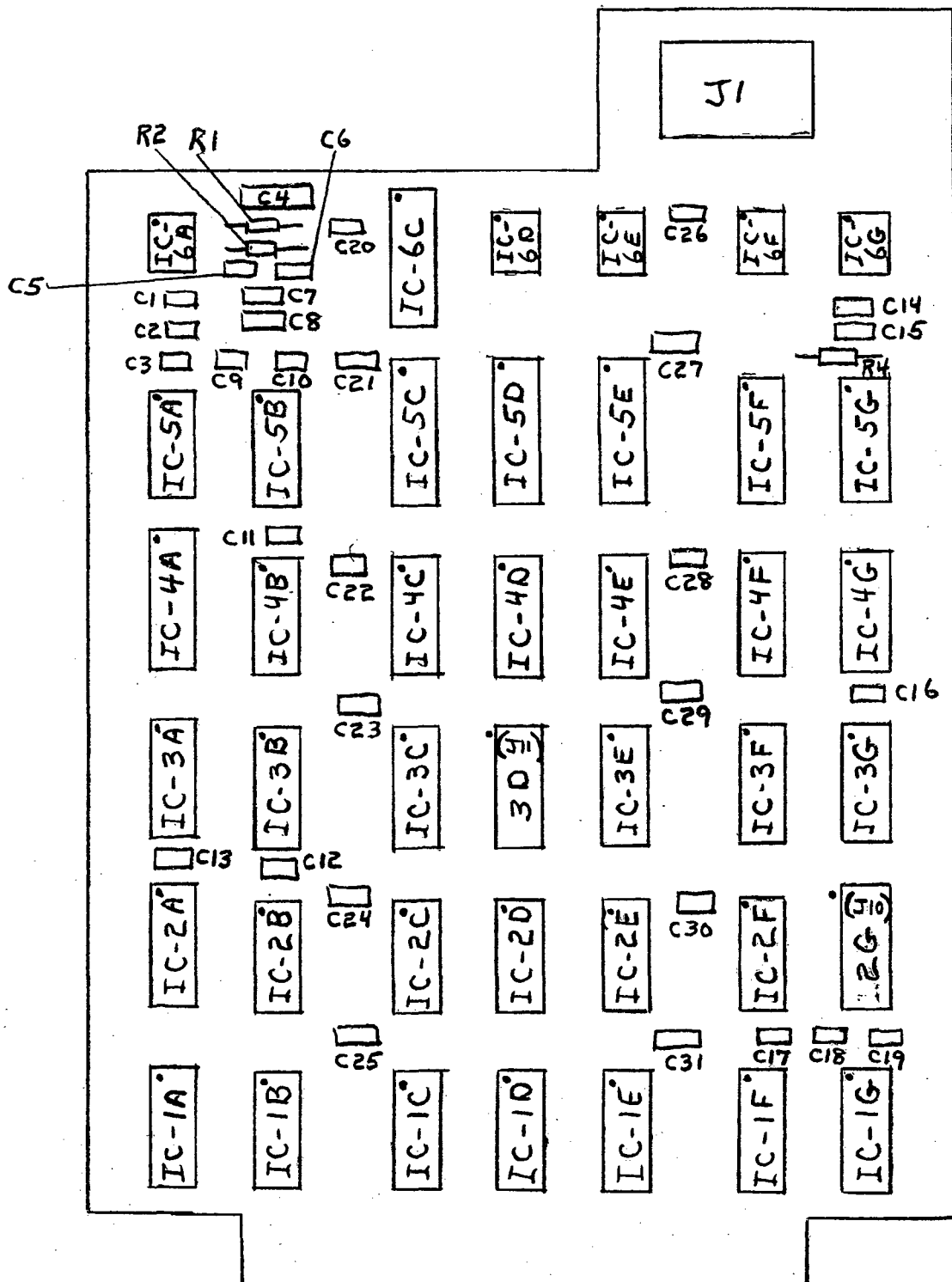
"Interface B" handles all information going to the keypads. One of its chief functions is to transmit address information which it receives via the "Address Bus" from the "Program & Address Generator" section.

The "Program & Address Generator" section, essentially a programmable up/down counter, determines the sequence of operations. Its address generator provides address information for both "Interface B" to the

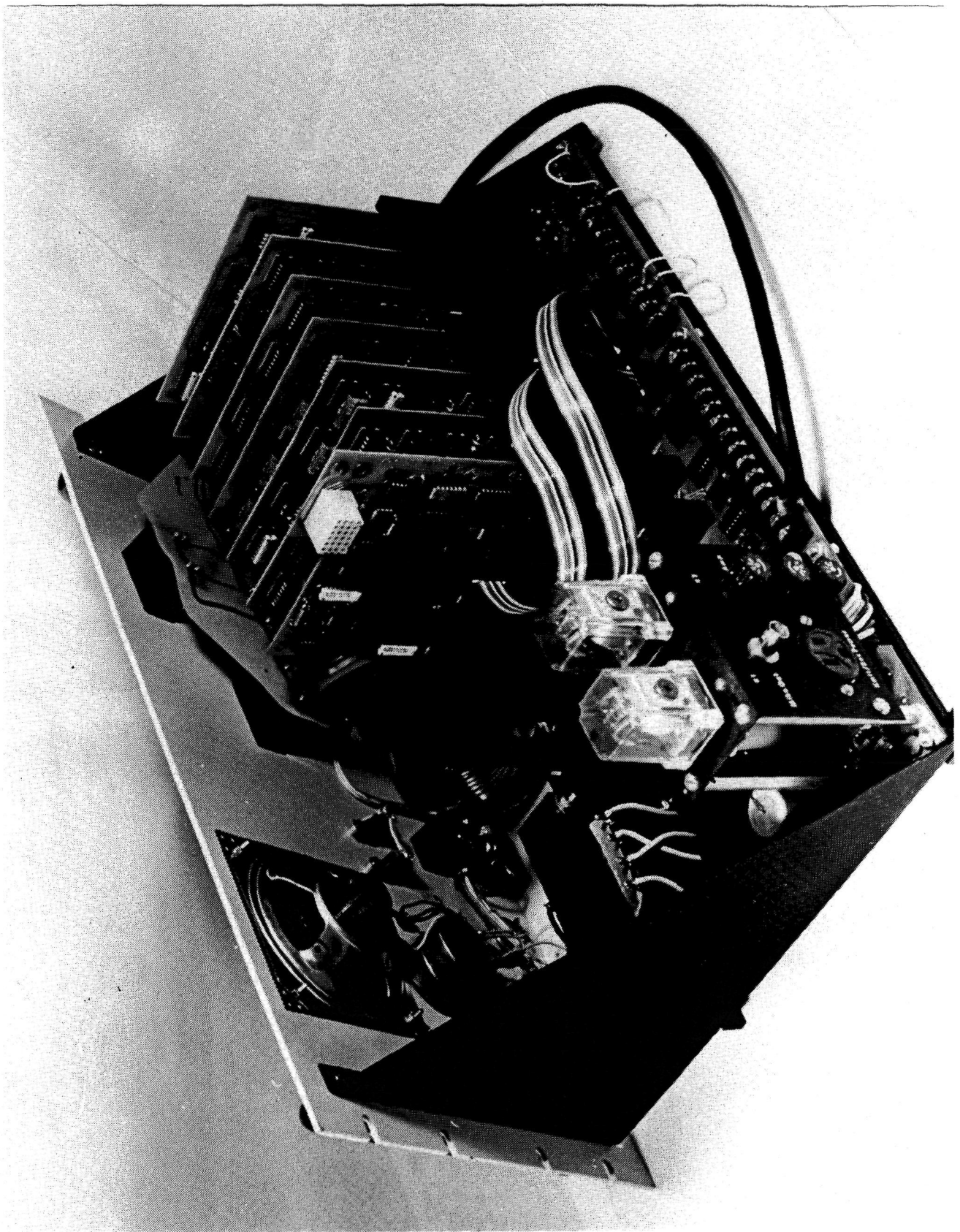


SYSTEM BLOCK DIAGRAM

FIGURE 5



POLEER BOARD LAYOUT
FIGURE 7



DIGITAL COORDINATOR, FIGURE 8

keypads, as well as to the memory.

The poller schematics are shown in figures 9 - 14. There are three distinct modes of operation of the poller:

1. Polling from the keypads with right/wrong feedback with a time of locking the entries into the pads.
2. Polling the keypads with no right/wrong feedback and no lock time.
3. Polling previously entered digits stored in the poller's internal memory.

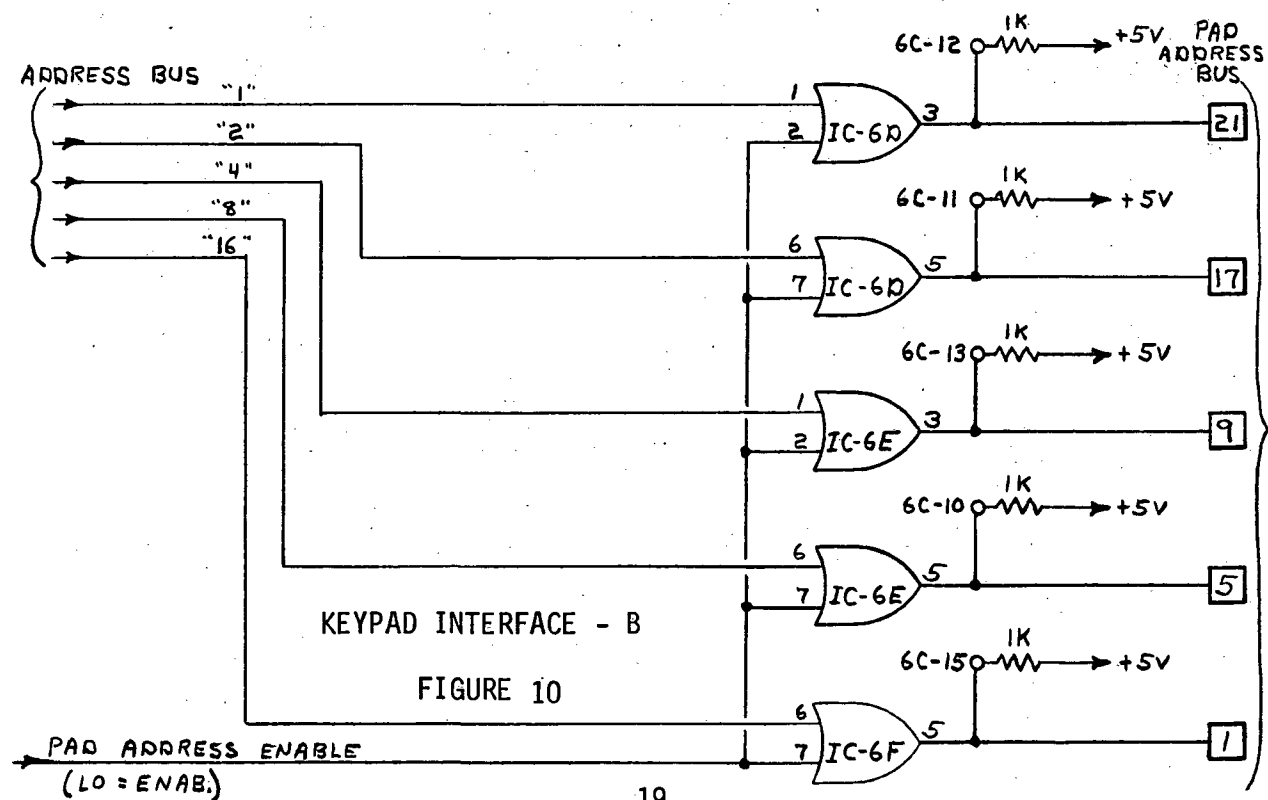
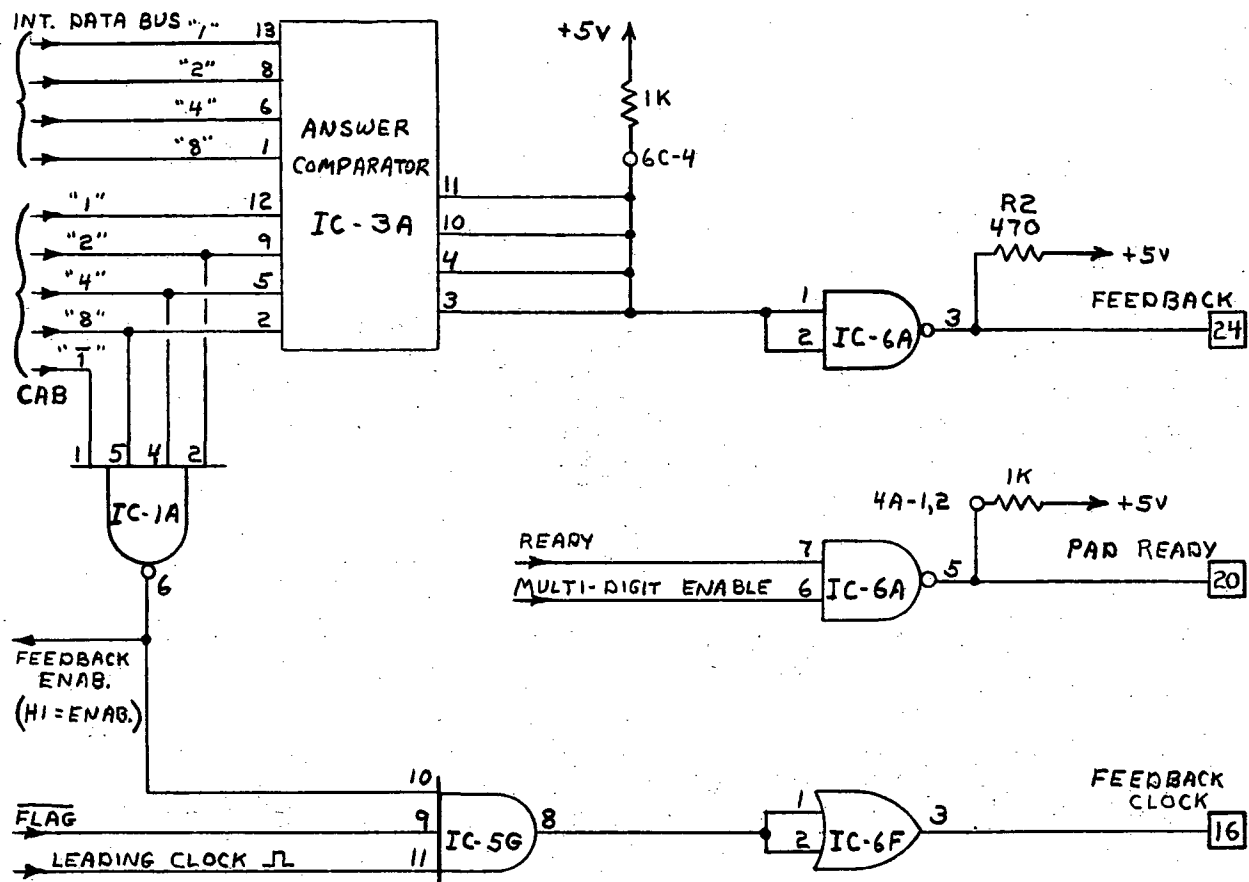
MODE 1

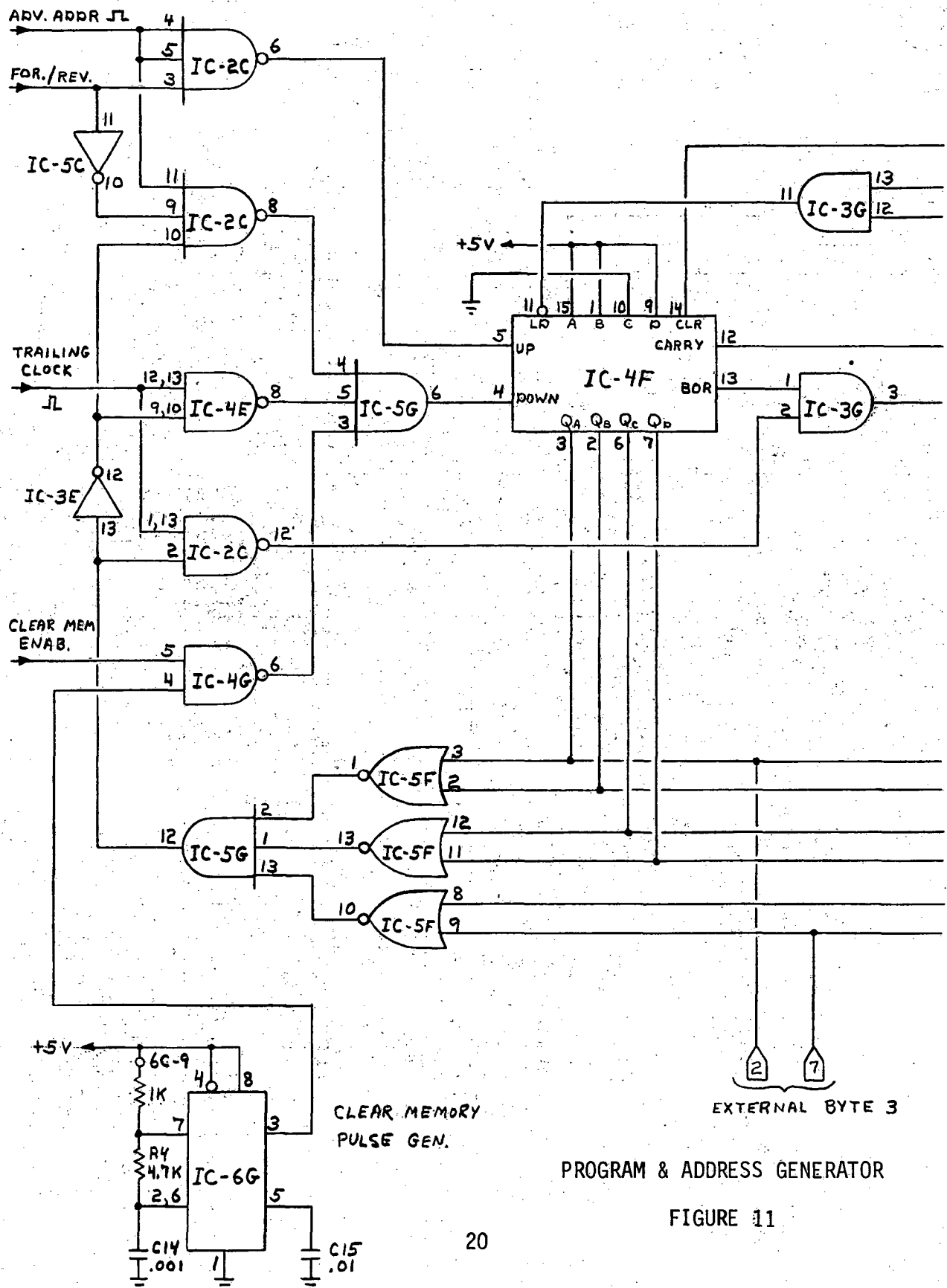
The sequence of operations in the first mode begins with the coordinator supplying 7 bits of information received from the network center to the RB3 (Received Byte 3) port (ref. fig. 9) along with an AR (Address Recognized) pulse. When the 7 information bits represent the code for "ready," NAND gate IC-1E presents a negative pulse on its output pin 8. This sets the READY LATCH, resulting in a low level on the "ready" line. This causes a high level output on pin 5 (ref. fig. 10) of driver IC-6A, which is fed to all the pads, lighting their "ready" indicators.

After a time (determined at the network center) another 7 information bits and an address recognized pulse are fed from the coordinator to RB3 and AR, respectively, (ref. fig. 9). If bits 1, 3, and 5 are logic "ones" (high levels), the NAND gate ($\frac{1}{2}$ of IC-1A) whose output at pin 8 feeds the GO LATCH will supply a negative "go pulse." The GO LATCH will be set giving a high level \overline{GO} and a low level GO output. Simultaneously the "go pulse," inverted at pin 10 of IC-3E, will clock information bits 0, 2, 4, and 6, representing the correct answer, into the CORRECT ANSWER REGISTER IC-2A.

The "go pulse" is also used at pin 11 of IC-3F and IC-4F to preset the counter in the "Program & Address Generator," and to form the beginning "preamble strobe." (Ref. fig. 11). In this latter respect the "go pulse" is fed to pin 5 of an AND gate from IC-3G. The pulse appears at output pin 6, input pin 4 being normally high, and passes through 2 of 4 inverters from IC-1F. The four inverters collectively form a 3 input OR gate. Since the other 2 inputs are low, and hence the gate is enabled, the "go pulse" appears at the output as the "preamble strobe" which is fed to the coordinator.

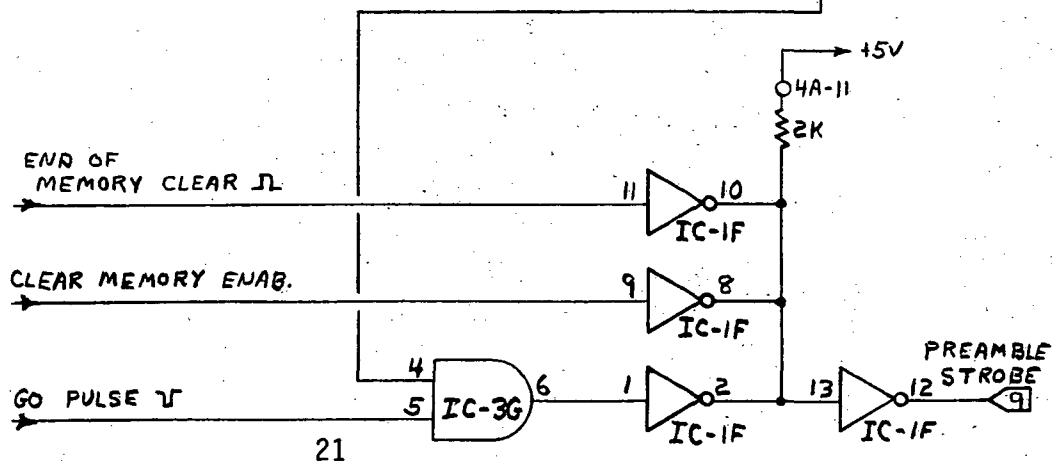
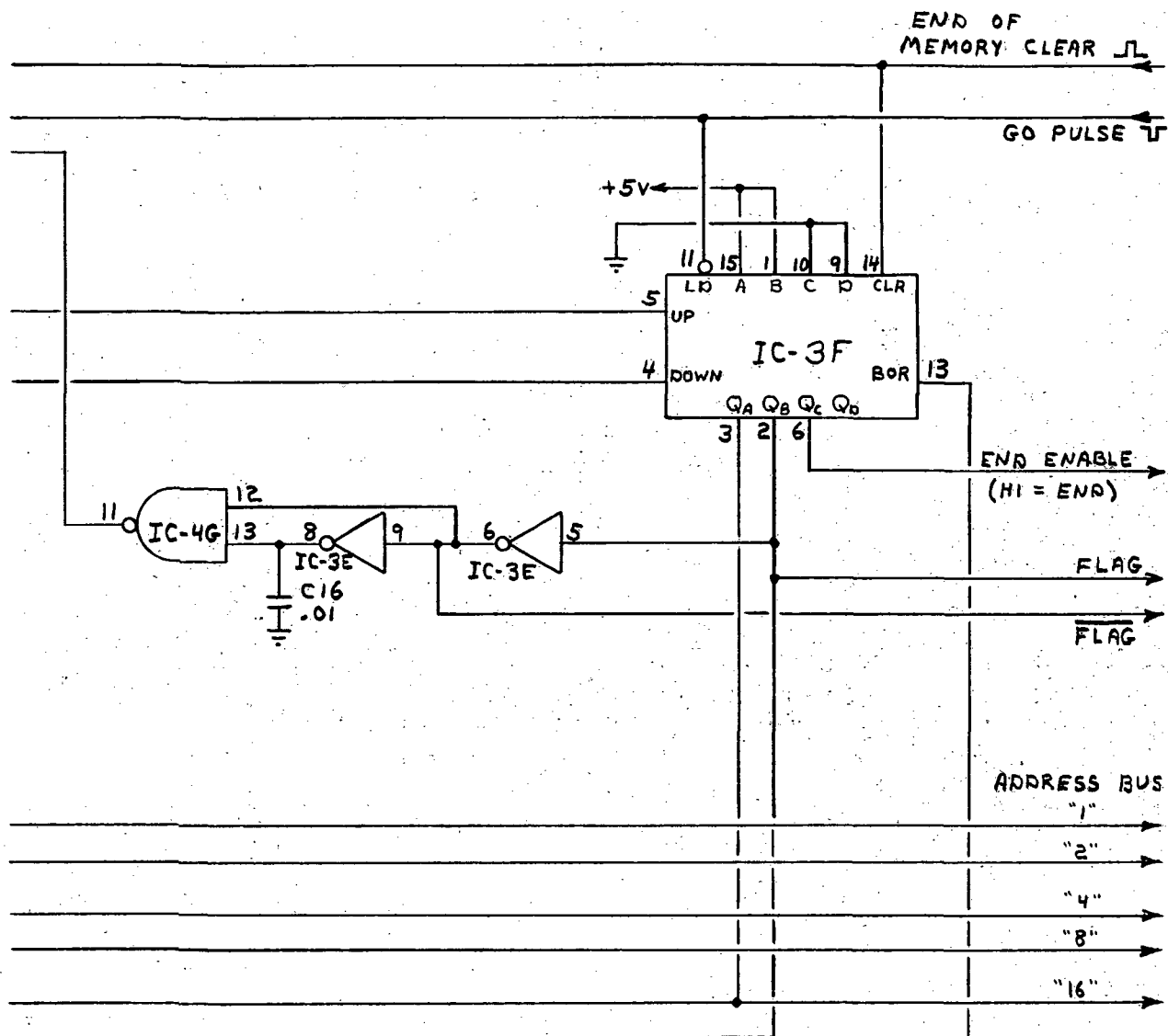
This strobe will cause the coordinator to transmit its preamble. However, the status information word in the preamble will be modified. This is accomplished by the poller applying its GO signal to the coordinator's SEB3 (Select External Byte 3) port. Since the GO signal is low, the external byte 3 will be selected. Two bits are presented

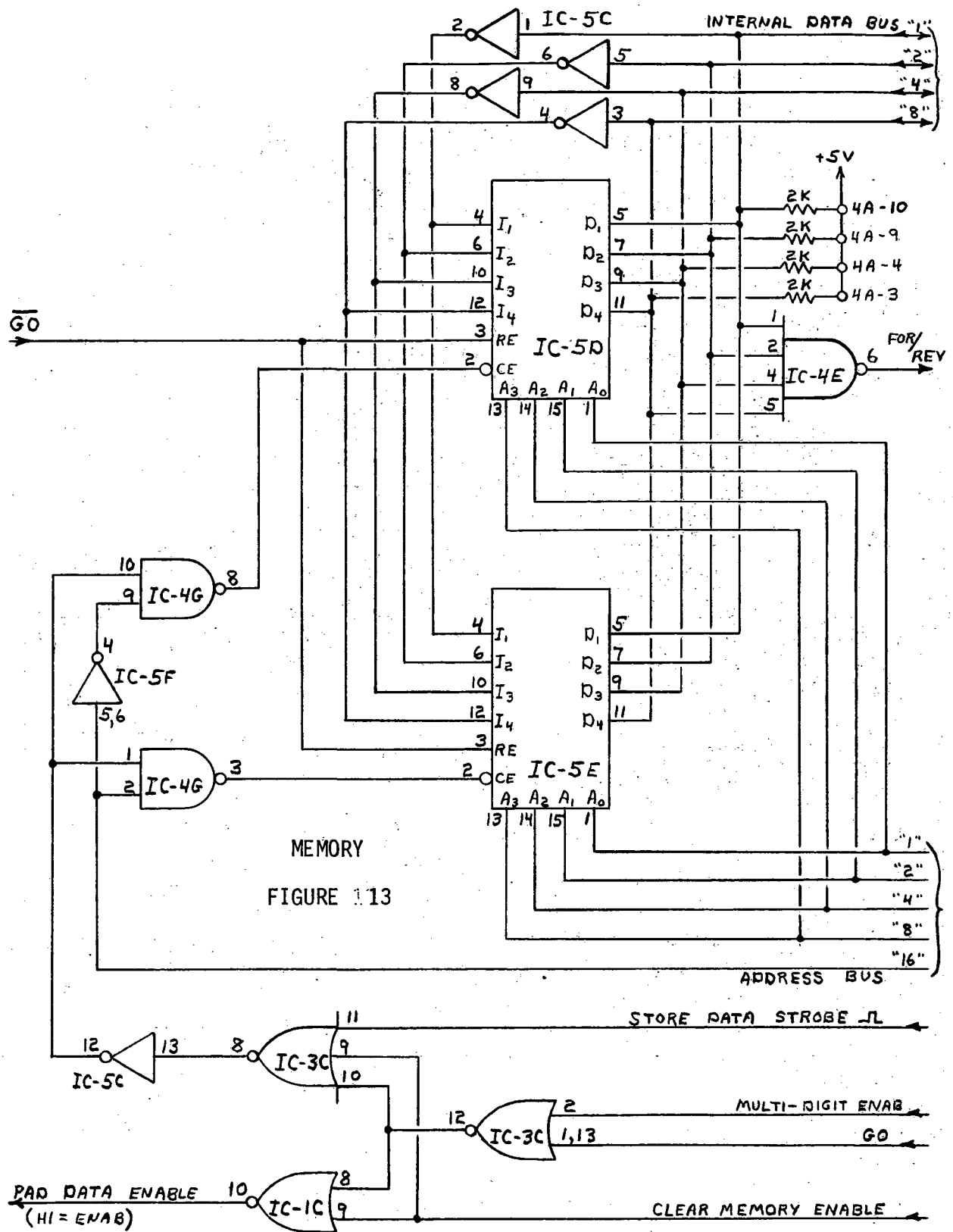


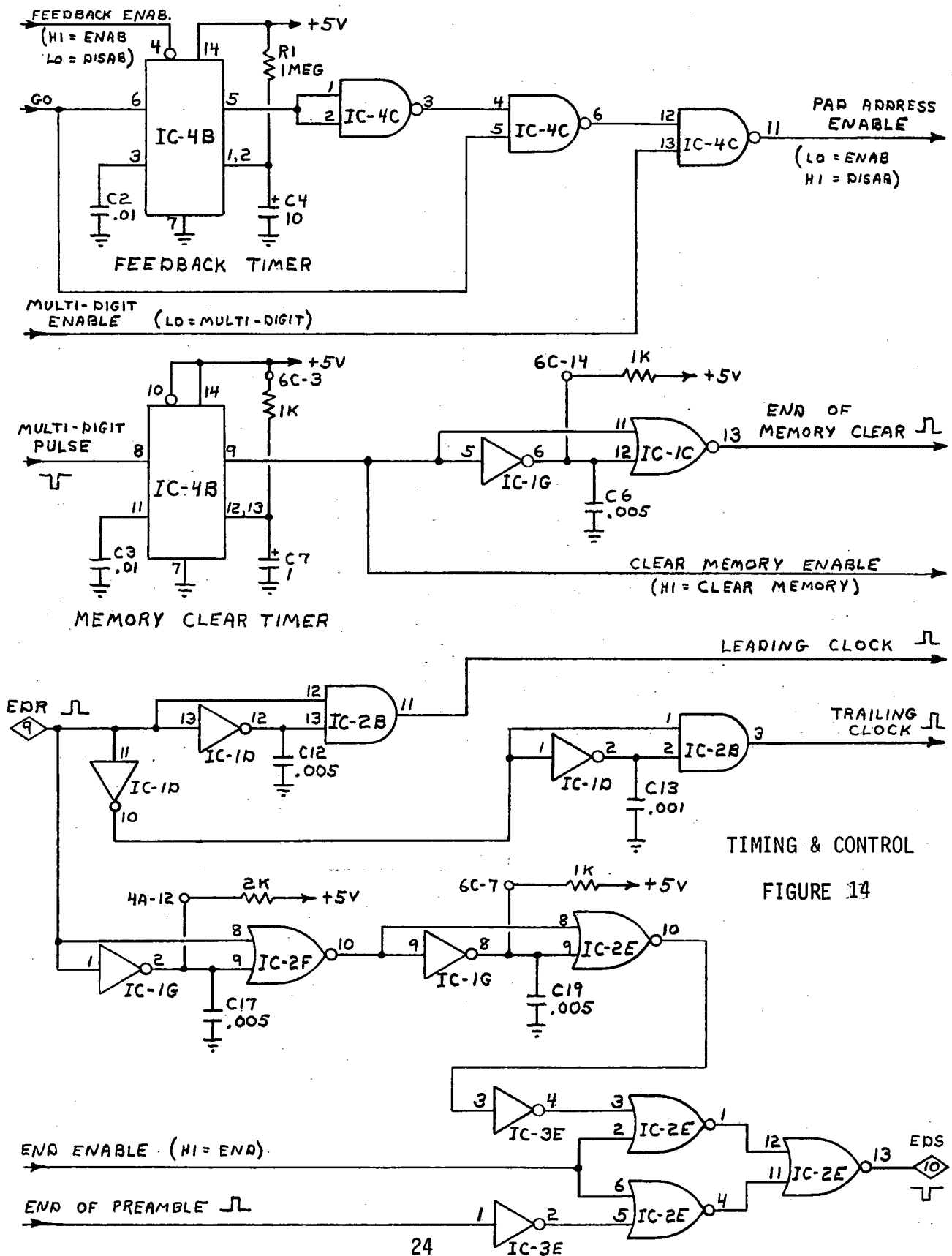


PROGRAM & ADDRESS GENERATOR

FIGURE 11







to this 7 bit EB3 (External Byte 3) port from the "Program & Address Generator" section (ref. fig. 11). The other 5 bits of the EB3 port are allowed to float at a high level. The two bits change from the beginning of the sequence to the end to differentiate between the preamble and postamble.

While the coordinator is transmitting the preamble it presents a high level \bar{D} signal to the poller. This signal, when applied to pin 1 of the three-state driver circuit IC-4D (ref. fig. 12), puts the drivers' outputs into the high impedance (open circuit) state. Thus the poller cannot interfere via the ED (External Data) port with the preamble data. When the \bar{D} signal returns low at the end of the preamble, the poller can present data to the coordinator via the ED port, since the GO signal at pin 15 is already low.

The low GO signal at pins 1 & 13 of IC-3C (ref. fig. 13) also results in a high "pad data enable" signal at IC-1C pin 10, since the "multi-digit enable" signal is normally low and the "clear memory enable" is normally high. When the preamble is finished and \bar{D} goes low, the "pad data enable," fed to the three-state buffer IC-5A (ref. fig. 12), allows data from the keypads at the PD (Pad Data) port to appear on the ED (External Data) port to the coordinator.

The end of the preamble is detected by feeding the \bar{D} signal to a negative edge detecting pulse generator. (Ref. fig. 9). This circuit, formed by an open-collector inverter from IC-1G, a NOR gate from IC-2F, a 1K resistor, and capacitor C18, supplies a positive "end of preamble" pulse at pin 4 of IC-2F. Since the "end enable" line is low at this time, the "end of preamble" pulse does not propagate through the following NAND gate from IC-2D. Instead it is allowed to pass through an inverter from IC-3E (ref. fig. 14) and two NOR gates from IC-2E to form the EDS (External Data Strobe) pulse to the coordinator.

This pulse causes the coordinator to transmit the data which is available at the ED (External Data) port (ref. fig. 12). Since the counters have already been preset to generate the initial keypad address (that of #28), data from that pad will be transmitted.

When the data word from keypad #28 has been transmitted, the coordinator will return an EDR (External Data Request) pulse to the Timing & Control section (ref. fig. 14). The leading (rising) edge and trailing (falling) edge are both detected by edge detecting pulse generators whose outputs at pin 11 and 3 of IC-2B form the "leading clock" and "trailing clock" pulses, respectively.

The "leading clock" pulse becomes the "feedback clock" pulse in the Interface B section (ref. fig. 10). It is gated through an AND gate from IC-5G, whose other inputs are the "flag" and the "feedback enable" signals. The "feedback clock" pulse to the keypads causes the right/wrong information on the "feedback" line to light the appropriate indicator on the individual keypad.

The "trailing clock" pulse is applied to the Program & Address Generator section (ref. fig. 11) where it is gated through a NAND gate from IC-4E and an AND gate from IC-5G to form the negative "down" clock pulse for the counter. The counter is made up of IC-4F and IC-3F. The four outputs of IC-4F and the Qa output of IC-3F provide information to the address bus. A negative pulse at pin 11 of either circuit presets that circuit's outputs to the state of its A - D inputs. The initial presetting (by the "go pulse") is such that the address bus sees a binary "27," Qb of IC-3F is high, and Qc & Qd are low.

As the "trailing clock" decrements the counter following transmission of each keypad's data, the counter steps from "27" to "0." The next pulse after arrival at the address "0" causes the transition of the Qb output of IC-3F from a high level to a low level and Qa from a low to a high level. This marks one complete pass in polling the 28 keypad locations. The Qb signal is inverted and its transition causes a negative pulse to be generated at pin 11 of IC-4G. This pulse passes through the AND gate from IC-3G to activate the pin 11 input of IC-4F. The resulting presetting of IC-4F, plus the fact that Qa of IC-3F has just gone high, brings the "address bus" from "0" back to "27" (binary).

Another full pass of polling all the keypads is now made. Since the "flag" and "flag" signals from Qb of IC-3F were high and low levels, respectively, during the first pass, the "flag" signal applied to pin 9 of IC-5G (ref. fig. 10) inhibited right/wrong feedback to the keypads. On the second pass, however, feedback is enabled. The "flag" signal forms one of the information bits which are fed to the coordinator's ED (External Data) port (ref. fig. 12). This provides information on which pass is being executed at any particular time.

In addition to triggering the "leading clock" and "trailing clock" pulses, the EDR (External Data Request) pulse (ref. fig. 14) has another function. Two negative edge detecting pulse detectors in series are triggered by the EDR pulse's trailing edge. After a time delay equal to the pulse width out of the first detector, the second detector's output at pin 10 of IC-2E presents a positive pulse which, inverted, becomes the next EDS (External Data Strobe) pulse. Thus the cycles continue from External Data Strobe to External Data Request, leading and trailing clocks, back to External Data Strobe, and so on.

When the counter in the Program & Address Generator section (ref. fig. 11) reaches binary "0" on the address bus at the end of the second pass, the level at pin 12 of IC-5G goes from low to high. This inhibits the next "trailing clock" pulse from clocking IC-4F, but enables it to pass from pins 1 & 13 of IC-2C through pin 2 of IC-3G to clock IC-3F. This causes all the outputs of IC-3F to go high, and results in a high level on the "end enable" line. The "trailing clock" gated to IC-3F also is internally gated to appear at output pin 13. From there it is gated through IC-3G and IC-1F to the "preamble strobe" output where it triggers transmission of the postamble.

The "end enable" signal is fed to the Timing & Control section (ref. fig. 14) where it inhibits the pulse triggered by the last EDR (External Data Request) pulse and the "end of preamble" pulse from triggering the EDS (External Data Strobe) line. The "end enable" signal is fed also to the Command Decoding & Latches section (ref. fig. 9) where it enables the "end of preamble" pulse to pass from pin 9 of IC-2D through pin 10 of IC-2B to reset the READY LATCH and GO LATCH. These latches were reset (cleared) when power was first applied to the coordinator by the negative $\overline{\text{POR}}$ pulse.

Following transmission of the postamble, the address (binary 16) on the address bus (ref. fig. 10) is enabled to remain active on the "pad address bus" for a period of approximately 15 seconds. This prevents the "unlock" signal from being generated in the keypads, and hence they remain locked with the right/wrong indication displayed. The end of this period is determined by the FEEDBACK TIMER in the Timing & Control section (ref. fig. 14). Its high output on pin 5 during the lock period holds the "pad address enable" line in the enabled condition. When the timer's output returns low, the keypads see all high levels on the address lines (ref. fig. 10), the keyboards are unlocked, and the displays extinguished.

MODE 2

Operation of the poller in the second mode (no right/wrong feedback and no lock time) is similar to that in the first mode. In this mode, however, the network center sends a special set of information bits (equivalent to a binary "14") to be entered into the CORRECT ANSWER REGISTER (ref. fig. 9). The 4 input NAND gate IC-1A (ref. fig. 10) decodes this information and presents a low output on its pin 6 as long as the special code is stored in the CORRECT ANSWER REGISTER. The low level output impressed on pin 10 of IC-5G disables any "leading clock" pulses from propagating to the "feedback clock" output. Thus no right/wrong indicators are turned on at the keypads. In addition the low "feedback enable" to pin 4 of IC-4B (ref. fig. 14) inhibits the FEEDBACK TIMER from being started by the GO signal. Therefore the keypads are unlocked as soon as the polling process is completed.

MODE 3

Mode 3 (multiple digits stored in the poller's memory) presents more dissimilarities with respect to mode 1. In this case a special "ready" command is sent from the network center. This command plus the AR (address recognized) pulse is decoded by the NAND gate IC-1B (ref. fig. 9). The resulting "multi-digit pulse" sets the MULTI-DIGIT LATCH, causing a low level signal on the "multi-digit enable" line. This signal applied to pin 6 of IC-6A (ref. fig. 10) activates the "ready" indicators at the keypads.

Meanwhile the "multi-digit pulse" triggers the MEMORY CLEAR TIMER (ref. fig. 14), initiating the sequence to clear previously stored data

from the memory. The high level "clear memory enable" applied to pin 5 of IC-4G (ref. fig. 11) allows pulses from the CLEAR MEMORY PULSE GENERATOR to clock the counter in the "down" mode. A sufficient number of pulses are allowed to pass to the counter that the address of each memory location is generated on the address bus at least once during the memory clear sequence. During the cycling of the counter it is likely that the state will be reached where the borrow output pin 13 of IC-3F will generate a negative pulse. To prevent this from triggering a false "preamble strobe" during or at the end of the memory clear sequence, the "clear memory enable" and the "end of memory clear" form inhibit inputs to the OR gate made up of four inverters from IC-1F.

The "clear memory enable" applied to the memory (ref. fig. 13) accomplishes two things. First it forces a low output at pin 10 of IC-1C, disabling the pad data buffer IC-5A (ref. fig. 12), keeping the "internal data bus" from being affected by any keypad entries. The "internal data bus" has high levels on all its lines due to the four pull-up resistors from circuit 4A pins 3, 4, 9, & 10 (ref. fig. 13). Secondly the "clear memory enable" applied to pin 9 of IC-3C forces a high signal at input pins 1 & 10 of IC-4G. This allows one of the memory circuits IC-5D & IC-5E to be enabled according to the state of the "16" line of the "address bus."

Since the \overline{GO} signal is low at this time the R_E (Read Enable) inputs of the memory circuits cause data to be written into the circuits while holding their outputs in a high impedance (open circuit) state. The high levels on the internal data bus are inverted by four sections of IC-5C. Thus the memories have all low levels written into all of their storage locations during the memory clear sequence.

The end of the clear sequence is evidenced by a positive pulse on the "end of memory clear" line (ref. fig. 14). This pulse is formed by a negative edge detecting pulse generator following the MEMORY CLEAR TIMER. In addition to inhibiting a false "preamble strobe," the "end of memory clear" pulse is applied to pins 14 (clear inputs) of IC-3F and IC-4F (ref. fig. 11). The resulting "0" (binary) on the "address bus" is the first memory address for data entry.

The "multi-digit enable" signal, which went to a low level at the beginning of the memory clear sequence, continues to be low. It is fed to pin 13 of IC-4C (ref. fig. 14) where it holds the "pad address enable" line in a disabled state. The keypads are therefore unlocked as a result of the high levels on all the "pad address bus" lines (ref. fig. 10). Any keypad may have a digit entered into it, but since no keypad from 0 to 28 (binary) is being addressed no data should ordinarily return to the poller. Nevertheless, data is desired at this point from some keypad for entry into the memory. This seeming conflict is resolved by giving keypad no. 28 (binary 27) a purposely ambiguous address. Through proper setting of its address switches it can be made to respond to either address code "11011" (binary 27) or "11111"

(binary 31). When the "pad address bus" is in the disabled, all high level state, only this keypad can present data to the poller for storage. It is also the only one that can return an MDEC (Multi-Digit Entry Clock) pulse.

The MDEC pulse is fed to two timers from IC-5B in the "interface A" section (ref. fig. 12). The first timer to time out (the upper one in the diagram) feeds a negative edge detecting pulse generator from IC-5B pin 5. The edge detector presents a positive pulse at IC-1C pin 4 at the end of the timer's interval which pulse becomes the "store data strobe."

Since the "clear memory enable" (ref. fig. 12, 13, 14) has now returned low, the "pad data enable" has returned high, and the data from the master pad (pad #28, binary #27) is present on the internal data bus. Since the memories read out bits that are inverted from those which have been written into the memories (ref. fig. 13), the data on the "internal data bus" is inverted by four stages of IC-5C before being written into the memories. The \overline{GO} signal is still low, and hence the memories are in the "write" mode. The "store data strobe" pulse through stages of IC-3C and IC-5C becomes the enable pulse which causes the keypad data to be entered into the memories.

The second timer in the "Interface A" section (ref. fig. 12) initiates another positive pulse at pin 1 of IC-1C which is the "advance address" pulse. This occurs after the "store data strobe" has entered the current keypad data into the memory. The "advance address" pulse, applied to pins 4, 5, & 11 of IC-2C (ref. fig. 11) will either increment (advance) or decrement (reverse) the counters, depending on the FOR/REV (Forward/Reverse) signal.

The FOR/REV signal (ref. fig. 13) is determined by the data from the master keypad on the "internal data bus." In every case but one the FOR/REV output from pin 6 of IC-4E will be a high level. This enables the counter in the "Program & Address Generator" to count up. (It should be noted that addresses are generated in the "up" mode--from binary "0" to "27"--for data storage. This is opposite to the "down" mode--from binary "27" to "0"--used for polling and transmission. The down mode is used for polling memory locations as well as the keypads. This difference in the directions of data entry and memory readout is easily handled by the computer at the network center, however.)

The one exception to this "up" data entry occurs when the keypad data are all high levels. This corresponds to an entry of the key marked # (displayed as F). By means of this function the # key on the master keypad becomes a special error correction key. Whenever this key is depressed during multi-digit data entry the counter will reverse to the previous storage address and new data can be entered in place of the erroneous data. Should a series of errors be made the # key can be depressed as many times as needed to cover all the errors.

When the # key has been depressed the FOR/REV (Forward/Reverse) signal goes low. This enables the "advance address" pulse to pass to the "down" input of the counter (ref. fig. 11) rather than to the "up" input. Should the down counting bring the "address bus" plus "flag" to "0" the zero detecting gates from IC-5F & IC-5G will generate a high level on pin 12 of IC-5G. This signal, after inversion, inhibits further down counting, preventing the counters from "end around" counting to all high levels. Thus the counter sits in the "0" state until an "up" pulse is received.

After allowing sufficient time for the operator to enter the data, the network center can initiate a polling command. The subsequent high GO signal puts the memories in the "read" mode, the low GO and the remaining low "multi-digit enable" disable the keypad data buffers by a low "pad data enable" signal, and polling from the memory now commences just as from the keypads.

4.0 DCOS OPERATION

4.1 NETWORK CENTER FUNCTION

The network center, with its on-line minicomputer, is the nerve center for DCOS operations. Its computer is charged with the tasks of addressing each site in order, collecting data in the appropriate mode from each site, and timing the occurrences of commands such that an orderly flow of data results. Along with these are the needs to present the proper modulation to the proper channel of the remote transmitter, selection of antenna, keying the transmitter, selection of receive frequencies, and other housekeeping tasks. The extent to which the computer software can automate the process and relieve an operator from manual intervention is a function of the predictability of the sequence desired. A copy of a versatile DCOS operating program for an HP-2100 has been delivered to NASA. This program requires a minimum of input from the network center operator while still giving him control of the process.

The sequence begins with the network center transmitting a "ready" command to each participating site. At this time the decision must be made whether the polling will cover data from the keypads or multiple digits stored in the site poller's memory by the master keypad.

Transmission of the command to poll is delayed by a time depending on the mode and circumstance of polling. If the multiple digit mode is used, a relatively long time may be desired, 5 to 15 minutes, for example, to allow the site operator to gather the data and enter it at his convenience. The delay in a right/wrong keypad mode might depend on the proper time allotted to the user to respond. In the no-feedback mode, useful for opinion or preference polling, the delay might be quite short, 5 - 10 seconds, for example.

After transmission of the proper polling command the data are received back at the network center. Should errors be noted by the computer, a request to repoll may be automatically sent. This allows for a "majority vote" to determine what data are most likely correct. The data may then be put in the desired format and displayed on a CRT screen, stored on tape or disk, and/or printed on paper.

4.4.2 SITE FUNCTION

The design of the system is intended to make the operation of the hardware as transparent to the user as possible. The only operating duties of the site personnel are effectively to turn on the equipment and enter data as appropriate. A certain amount of education is required of the users regarding the right/wrong and ready indicators and the timing of data entry according to the ready indicator. The pocket calculator, to which the keypad is similar, has become so ubiquitous that user acceptance and familiarity is unlikely to be a problem.

The keypads have been purposely made to be in the unlocked mode for the majority of the time. Hence users can enter data and modify their entries, simultaneously viewing their entry on the keypad display, at nearly any time. This allows the user to become accustomed to the keypad even when the system is not being addressed by the network center.

One setup function which might occasionally be required at the site is addressing or readdressing of a keypad. The directions for this are simple and are included in the appendix.A.

The site operator must be instructed with the procedure for multiple digit entry from the master keypad. Care must be exercised in entering the digits in the proper order. Use of the # key backs up the address and allows a correction of the last entry made, while multiple use of the # key backs up the address by the number of times the key is depressed. Diligence in noting how many digits have been entered as well as how many back up steps have been made is required of the operator.

5.0 DCOS FIELD TESTING & USE

Difficulties with the VHF system caused a shortage of personnel during the developmental period of the DCOS. In addition, material procurement and redesign delays together with the resignation of the staff computer programmer impacted heavily on the DCOS schedule. Consequently a working model was not taken to the field until April of 1975.

On April 28 and 29 tests were performed on a DCOS system installed at Saratoga, Wyoming. Two-way data tests showed the system to be capable of receiving commands via the ATS-3 satellite and in turn

transmitting valid data back over the link. In these tests only one keypad was used. Valuable information regarding improvements to the computer program was obtained.

On May 14, 1975 twelve additional keypads were operated in the system. Using an improved computer program allowing more automatic operation, the test involved operation coordinated with actual on-the-air ATS-6 broadcasting. Twelve students participated in responding to questions displayed on the ATS-6 video monitor. Both the right/wrong and opinion (no feedback) modes were used. The test was very successful both in regard to the students' enthusiastic acceptance and the valid data returned over ATS-3.

The end of the STD programming and the move of the ATS-6 satellite to India prohibited further testing of the above nature. However, on July 16, 1975 a VHF-only test over ATS-3 was done with a site configuration at Goddard Space Flight Center. Reception at Denver once again verified the satisfactory operation of the system.

6.0 RESULTS, CONCLUSIONS, & RECOMMENDATIONS

The May 14 test at Saratoga with 12 students using the keypads had the rest of the class as a control group. The results indicated the students with the keypads showed more attention, comprehended the material better, and indicated more positive acceptance of the program than those without keypads.

Interest from other sites not equipped with the DCOS system was evidenced by questions over the VHF audio link. This prompted a brief explanation of the system in return over the ATS-6 video channel.

The system, although not tested as extensively as originally planned, can be concluded to be of value both as a means of rapid data acquisition from diverse sources, and as a potential tool of great versatility for educational purposes.

It is recommended that both the data acquisition and educational phases be pursued with respect to further applications.

Educationally it is unique in that it not only measures a student's comprehension, but due to its interactive nature it stimulates the student's interest in both the material and its means of presentation.

Particularly challenging would be a modification of the system which would present material to the student over the same digital link using a dot matrix or CRT display either individually or to the group. Presentation of the material, questioning of the users, collection of the answers, plus immediate analysis and modification of the program material could be all performed by the network center computer. Profiles of an individual participant's comprehension,

as well as his interest and acceptance, could be done by the computer on the basis of the responses. Furthermore, this could be done for large, scattered groups of users.

Any redesign effort would do well to consider the potential advantages of microprocessor technology.. It is likely that a microprocessor could integrate the functions of both the digital coordinator and the DCOS poller into one composite unit. Significant hardware reductions, cost savings, and increased reliability are likely to result with respect to the present collection of discrete logic circuits.

To improve the usefulness of the system as a data acquisition tool, some means to step through and display the contents of the multi-digit memory at the site could be added. This function, under the control of the site operator, would provide a means of verifying whether or not the stored data were correct. The present correction feature could then be used as needed.

APPENDIX A

At the initial installation of a series of keypads it will be necessary to assign addresses to each keypad. The addressing procedure described below should be performed exactly as described. Deviation from this procedure could result in damage to the keypad.

1. When initially installing the keypads to the cables, it is essential that all power to the digital coordinator and to the keypads be turned off.
2. Remove the cover of each keypad by removing the four screws that hold the rubber feet on the bottom of the case.
3. Observe the ten miniature rocker arm switches mounted in the red housing which is located just above the WRONG/READY/RIGHT and the Display indicators. Set all ten of the switches to the OPEN position by depressing the lower portion of each rocker arm. A ball point pen or similar blunt-pointed instrument is ideal for this purpose.
4. Each keypad should then be assigned a unique address. At this point, care should be taken that each address is assigned to one and only one keypad at a given installation. An address is assigned by operating to the ON position ONLY those rocker arm switches listed in Table I for the desired address. It is imperative that this be followed exactly to avoid possible component damage in the keypad.
5. When the keypads have all been assigned their address designations, they may be connected to the system cables.
6. Replace the top cover that was removed in step 2 above, securing with the screws that hold the 4 rubber feet in place. At this time, it would be well to mark the rear of the keypad case between the cable entry holes with the address designation to quickly identify what address has been assigned to that particular pad.
7. NOTE: Only four rocker switches are turned on for keypad #28 in order that it may function as the master keypad for multi-digit entry as explained on pages 28 and 29.

TABLE I

<u>Pad Address Designation</u>	<u>Turn "ON" Rocker Switches</u>
1	2 4 6 7 9
2	2 4 6 7 10
3	2 4 6 8 9
4	2 4 6 8 10
5	2 4 5 7 9
6	2 4 5 7 10
7	2 4 5 8 9
8	2 4 5 8 10
9	2 3 6 7 9
10	2 3 6 7 10
11	2 3 6 8 9
12	2 3 6 8 10
13	2 3 5 7 9
14	2 3 5 7 10
15	2 3 5 8 9
16	2 3 5 8 10
17	1 4 6 7 9
18	1 4 6 7 10
19	1 4 6 8 9
20	1 4 6 8 10
21	1 4 5 7 9
22	1 4 5 7 10
23	1 4 5 8 9
24	1 4 5 8 10
25	1 3 6 7 9
26	1 3 6 7 10
27	1 3 6 8 9
28	1 3 8 10

APPENDIX B

Integrated Circuits used in the keypad:

IC-1	7410	Fairchild	IC-11	7474	Fairchild
IC-2	7404	Fairchild	IC-12	9368	Fairchild
IC-3	899-1-R2.0K	Beckman	IC-13	7404	Fairchild
IC-4	7414	Texas Inst.	IC-14	7400	Fairchild
IC-5	7433	Texas Inst.	IC-15	899-1-R2.0K	Beckman
IC-6	7433	Texas Inst.	IC-16	7414	Texas Inst.
IC-7	7430	Fairchild	IC-17	7433	Texas Inst.
IC-8	7475	Fairchild	IC-18	7433	Texas Inst.
IC-9	DM8093	National			
IC-10	FND500	Fairchild			

Integrated Circuits used in the poller:

IC-1A	7420	Fairchild	IC-4B	NE556A	Fairchild
IC-1B	7430	Fairchild	IC-4C	7400	Fairchild
IC-1C	7402	Fairchild	IC-4D	DM8095	National
IC-1D	7404	Fairchild	IC-4E	7420	Fairchild
IC-1E	7430	Fairchild	IC-4F	74193	Fairchild
IC-1F	7405	Fairchild	IC-4G	7400	Fairchild
IC-1G	7405	Fairchild	IC-5A	74126	Texas Inst.
IC-2A	7475	Signetics	IC-5B	NE556A	Fairchild
IC-2B	7408	Fairchild	IC-5C	7404	Fairchild
IC-2C	7410	Fairchild	IC-5D	DM7489	National *
IC-2D	7400	Fairchild	IC-5E	DM7489	National *
IC-2E	7402	Fairchild	IC-5F	7402	Fairchild
IC-2F	7402	Fairchild	IC-5G	7411	Fairchild
IC-3A	9386	Fairchild	IC-6A	75452	Motorola
IC-3B	7400	Fairchild	IC-6C	898-1-R1.0K	Beckman
IC-3C	7427	Fairchild	IC-6D	75453	Fairchild
IC-3E	7404	Fairchild	IC-6E	75453	Fairchild
IC-3F	74193	Fairchild	IC-6F	75453	Fairchild
IC-3G	7408	Fairchild	IC-6G	NE555V	Fairchild
IC-4A	898-1-R2.0K	Beckman			

* Do not use 7489's from any other vendor for IC-5D & IC-5E.
For other 7400 series I.C.s other manufacturers may be used.